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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,004	04/07/2004	Yuan-Kun Hsiao	VOSP0002USA	3003

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EXAMINER	
SINGH, HIRDEPAL	
ART UNIT	**PAPER NUMBER**
2609	

NOTIFICATION DATE	DELIVERY MODE
05/23/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,004	HSIAO, YUAN-KUN	
	Examiner	Art Unit	
	Hirdepal Singh	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/25/2005, 11/07/2005, 8/29/2006, 9/05/2006, 9/12/2006, 4/16/2007.

DETAILED ACTION

This action is in response to the original filing date of April 07, 2004. Claims 1-20 are pending and have been considered below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 12, 13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Chou et al. (US 7,016,277).

Claims 1, 12, and 15: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal (abstract; column 1, lines 10-12; figure 5) comprising;

a. calculating the number of periods of reference clock according to the input wobble signal, calculating the average number from the counted number of periods to generate a control signal (column 3, lines 35-50; column 5, lines 7-26);

b. a phase locked loop PLL for generating a target/write clock signal according to the control signal, feeding the target clock signal back to the phase detector and generating the target clock signal according the control signal (column 6, lines 25-44);

c. the controller generates the control signal based on the adjustment value and the logic level of the average signal as shown in figure 6 (column 5, lines 18-27);

d. the phase detector is generating a control voltage for the low pass filter (the reference does not talk about the loop filter, but it is inherent that the Phase locked loop has a loop filter between voltage controlled oscillator and the phase detector);

c. controlling the frequency of the target clock based on the control voltage (column 5, lines 51-57).

Claims 2, and 13: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claims 1, 12, and 15 above, and further discloses that the circuit comprises;

a. reference clock generator generating a reference clock having predetermined frequency (column 4, lines 25-32);

b. a counter connected to reference clock generator counting the number of period according the input or wobble signal (column 4, lines 45-50);

c. a mean or average unit for calculating the average of count number (column 5, lines 22-26);

d. a controller which generates a control signal according to the average value and the rectification value is doing the same function as the comparator in the claimed invention (column 4, lines 22-37).

Claim 3: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claim 1 above, and further discloses that clock generator comprises;

a. a phase detector with wobble signal and the control signal as input and the second synchronization signal as another input, and generating a control signal according to the inputs (figure 5; column 4, lines 25-37);

b. the phase detector generating a control voltage for the low pass filter (the reference does not talk about the loop filter, but it is inherent that the Phase locked loop has a loop filter between voltage controlled oscillator and the phase detector);

c. a voltage controlled oscillator controlling the frequency of the target clock based on the control voltage (column 5, lines 51-57).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-9, 11, 14, 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US 7,016,277).

Claims 6, and 18: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claims 1, and 15 above, but does not explicitly disclose that when difference between count value and the average value is less than a critical value first control signal is set to a first logic level. However, Chou discloses that when the phase difference between ATIP (absolute time in pre-groove) signal and encoded sub code frame synchronization signal is less than a predetermined value the reference clock is the write clock signal (abstract; column 3, lines 46-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the count value and average value of the Chou device and compare the difference with a predetermined value to decide the logic level of the control signal. One would have been motivated to use the count value and average value to decide the logic level of control signal so that the generated clock signal from the PLL is in the correct phase.

Claims 7, and 19: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claims 1, and 15 above, but does not explicitly disclose that when difference between plurality of consecutive period count values and the average value are less than a critical value first control signal is set to a first logic level. However, Chou discloses that when the phase difference

between ATIP (absolute time in pre-groove) signal and encoded sub code frame synchronization signal is less than a predetermined value the reference clock is the write clock signal (column 3, lines 46-55), and further discloses that the first reference synchronization signal is generated based on the average value of plurality of count values which in turn controls the PLL (figure 5; column 3, lines 56-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the difference between plurality of consecutive period count values and the average value of the Chou device and compare the difference with a predetermined value to set the logic level of the control signal. One would have been motivated to set the logic level of control signal according to the difference between plurality of consecutive period count values and the average value to generate clock signal that is in the correct phase.

Claims 8, and 16: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claims 1, and 15 above, but does not explicitly disclose that when difference between period count value and the average value is larger than a critical value first control signal is set to a second logic level. However, Chou discloses that when the phase difference between ATIP (absolute time in pre-groove) signal and encoded sub code frame synchronization signal is less than a predetermined value the reference clock is the write clock signal (abstract; column 3, lines 46-55). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the count value and average

value of the Chou device and compare the difference with a predetermined value and set the logic level of the control signal to a second logic level if the difference is large or smaller than the predetermined value. One would have been motivated to use the difference between period count value and average value to set the logic level of control signal to a second logic level if the difference is larger than a predetermined value so that the generated clock signal is in the correct phase and does not get altered during the phase modulated cycles of the wobble signal.

Claims 9, and 17: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claims 1, and 15 above, but does not explicitly disclose that when difference between plurality of consecutive period count values and the average value is larger than a critical value first control signal is set to a second logic level. However, Chou discloses that when the phase difference between ATIP (absolute time in pre-groove) signal and encoded sub code frame synchronization signal is less than a predetermined value the reference clock is the write clock signal (abstract; column 3, lines 46-55), and further discloses that the first reference synchronization signal is generated based on the average value of plurality of count values which in turn controls the PLL (figure 5; column 3, lines 56-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the count value and average value of the Chou device and compare the difference with a predetermined value and set the logic level of the control signal to a second logic level if the difference is large than the predetermined value.

One would have been motivated to use the difference between period count value and average value to set the logic level of control signal to a second logic level if the difference is larger than a predetermined value so that the generated clock signal is in the correct phase and does not get altered during the phase modulated cycles of the wobble signal.

Claims 11, and 20: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claims 1, and 12 above, and further discloses that clock generating device may be applied to an optical disc drive as CD-RW (column 1, lines 15-26), and also discloses that the optical disc recorder simultaneously generate the encoder frame synchronization signal corresponding to each ATIP (absolute time in pre-groove frame) (column 2, lines 9-21), but does not explicitly disclose that a second control signal is generated to prohibit the PLL to synchronize the target clock with the input signal at a predetermined time. However, it is inherent that the absolute timing of the input signal is used to prevent PLL to synchronize the target clock with the input signal at a predetermined time. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to prohibit the PLL from synchronizing the target clock with the input. One would have been motivated not to synchronize the target clock with the input signal at a predetermined time to keep the signal from being unstable.

Claim 14: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claim 13 above, and further discloses generating an average value based on the period count value, but does not explicitly disclose that when average value equals an initial value the comparison between average and count value stops. However, it is inherent that the average value processor stops comparison with a predefined condition whether it is when the count value becomes equal to the average value. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to generate control signal based on the comparison and stop the comparison as a predefined condition is met. One would have been motivated to use the comparison of average and periods count values to generate the control signal and stop comparing when the period count value equals the average value.

5. Claims 4, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US 7,016,277) in view of Okamoto et al. (US 6,587,417).

Claim 4: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claim 3 above, but does not explicitly disclose that the clock generating device has second slicer. However, Okamoto discloses a similar method and device for clock generation and further discloses that the device includes slice signal processing unit (abstract; figure 14; column 15, lines 20-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to use the slicer in Chou device to select the level of input signal. One would have been motivated to use the slicer in the PLL circuit to get the target signal and input signal having similar wave forms.

Claim 10: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claim 1 above, but does not explicitly disclose that the clock generating device has a band pass filter. However, Okamoto discloses a similar method and device for clock generation and further discloses that the device includes a band pass filter and the output of the band pass filter is fed to the level slicer (abstract; figure 13; column 15, lines 20-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the band pass filter and slicer in Chou device to select the frequency and level of input signal. One would have been motivated to use the band pass filter and slicer at the input of clock generator to get the controlled input signal with limited amplitude and frequency.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US 7,016,277) in view of Hsu et al. (US 6,754,147).

Claim 5: Chou discloses a method and device for generating a clock signal using a wobble signal i.e. a phase modulated signal as in claim 1 above, but does not explicitly disclose that the clock generating device has a charge pump circuit for controlling the

control voltage from the phase detector. However, Hsu discloses a similar method and device for clock generation and further discloses that the PLL includes charge pump for controlling the voltage based on the phase detection (figure 16; column 1, lines 28-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a charge pump circuit with the loop filter in the PLL to generate the control voltage. One would have been motivated to use the charge pump included in the PLL circuit to generate the control voltage.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Eom (US 7,046,598) discloses a method and apparatus for detecting phase difference between reference and wobble signal.

b. Van vlerken et al. (US 6,765,861) discloses a method and apparatus for scanning the record carrier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hirdepal Singh whose telephone number is 571-270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off)8:00AM-5:00PMEST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Myhre can be reached on 571-272-6722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HS
5/14/07

James W. Myhre
Supervisory Primary Examiner